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OCR A Level Computer Science H446 – Paper 1

2

Processor performance

Unit 1

Components of a computer and their uses

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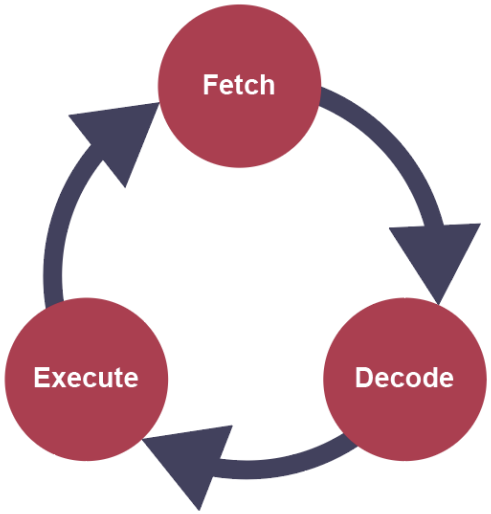
Objectives

- Describe the factors affecting the performance of the CPU: clock speed, number of cores, cache
- Understand the use of pipelining in a processor to improve efficiency

Fetch-execute cycle

- In the last lesson we looked at the fetch-execute cycle



- How do the machine code instructions relate to assembly language programs?

Words

- Memory is divided up in equal units called words
  - Word length is usually 8, 16, 32 or 64 bits
- Each word has a separate memory address
  - What would be the memory capacity in bytes of a machine with an 8-line address bus and a word length of 8 bits?

Address	Data or instruction
00000000	01101001
00000001	01101100
00000010	
00000011	10011111

Address bus

- The width of the address bus determines the maximum possible memory addresses of the system
- With an 8-bit address bus, the maximum number of memory addresses is $2^8 = 256$
- An average PC has a memory capacity of 4 GiB (gibi bytes), which is 2^{32} bytes
- Therefore, it must have a 32-bit address bus

Data bus

- The data bus is bi-directional as data can be sent both ways along the bus
  - The width of the data bus is defined by the number of wires
    or lines it contains
- If the data bus is the same width as a computer word, data can be transferred to and from memory in a single operation

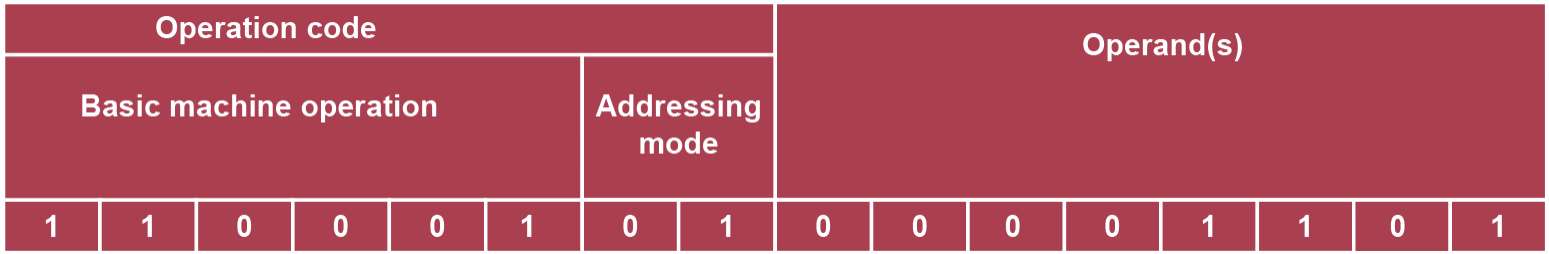
Format of instructions

- Assembly language is very closely related to machine code
  - Generally, there is a one-to-one correspondence between a machine code instruction and its assembly language equivalent
- The architecture of a computer, including
  - the word size
  - and the width of the address bus

  determine the format of a machine code instruction for a particular type of processor

A machine code instruction

- The basic structure of a machine code instruction is shown, and given below in



C50D ;load contents of accumulator into location 0B

- The equivalent assembly code instruction could be:

LDA #13

- The maximum size of the operand will depend on the width of the address bus

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Factors affecting performance

The main factors affecting processor performance are:

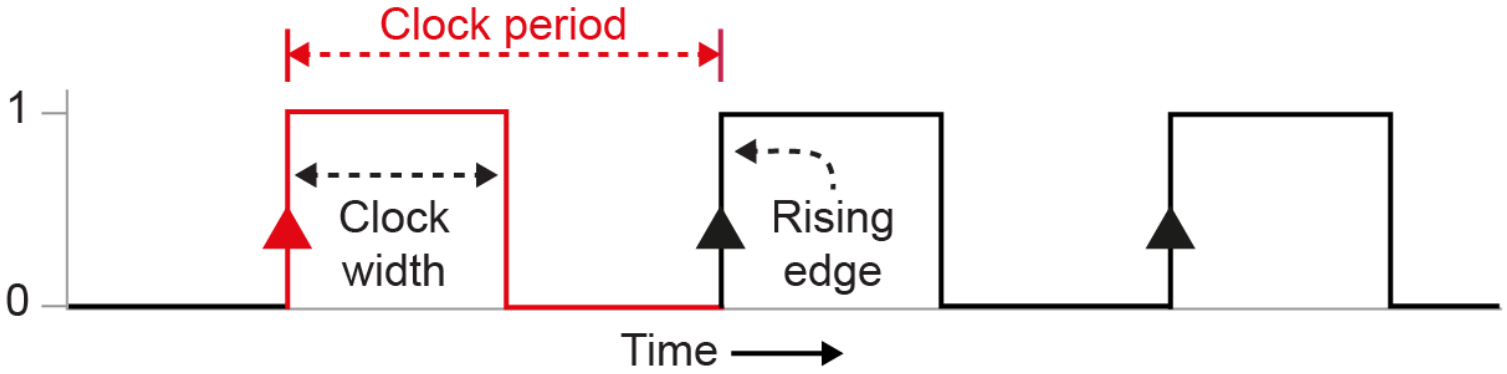
- Clock speed
- The number of cores in the processor
- The amount and type of cache memory

Factors affecting performance

- The Fetch-Execute cycle is triggered by the clock pulses of the system clock
- The faster the clock speed, the faster a computer can fetch, decode and execute instructions
  - This clock can change state many billions of times per second
  - A 4GHz processor would tick 4 billion times per second

The system clock

- A series of regular ON/OFF signals are used to synchronise the operations of the processor components
  - Actions are usually carried out on the rising edge of the clock
  - Actions each take a fixed number of cycles to



Number of cores

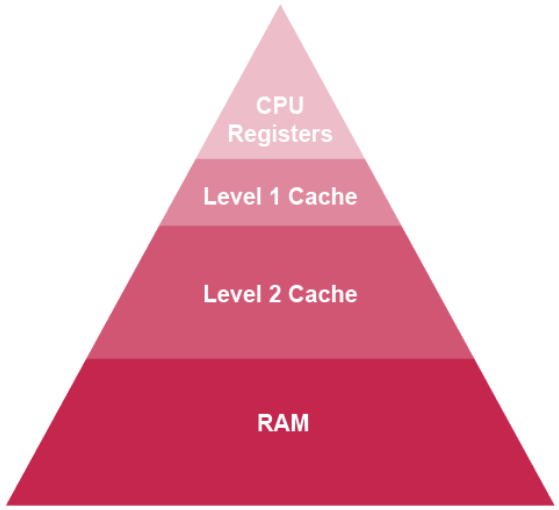
- Many computers today, including personal computers, have multiple cores
  - A dual-core computer has two processors linked together in the same integrated circuit
  - A quad-core computer has four linked processors
- Each core is theoretically able to process a different instruction at the same time with its own fetch-execute cycle, making a quad-core computer **two** or even **four** times faster than a single-core computer
  - However, the software may not always be able to take full advantage of all four processors

Parallel processing

- Using several processor cores working at the same time is known as parallel or concurrent processing
  - In systems designed for parallel processing, each core can work concurrently on different parts of the same task
  - Since instructions are processed sequentially, this is not always possible

Cache memory

- Cache is a small amount of superfast (but expensive) memory that stores data and instructions that have recently been used by the processor
  - Level 2 cache is larger but not as fast as Level 1 cache
  - Both types are [illegible] chip



Cache memory

- Level 1 cache memory is split into instruction cache and data cache, so that data and instructions can be fetched simultaneously
- The more cache memory a computer has, the more likely it is that it will not have to fetch the next instruction or data from RAM, as it will already have been loaded into the superfast cache memory from which it can be retrieved much more quickly

Pipelining

- This is a technique used to improve performance, for example by overlapping stages in the fetch-execute cycle, or by breaking down the stages in an arithmetic instruction
  - An instruction enters the pipeline, and as soon as one stage has been completed, another instruction enters the pipeline
  - A third instruction then enters before either of the others is completed
- There may be 10 or 12 stages in the pipeline, with some stages taking longer than others

Worksheet 2

- Complete the questions in **Task 1** on **Worksheet 2**

Plenary

- The three main factors affecting the performance of the CPU are:
  - Clock speed
  - Number of cores
  - Size and type of cache memory
- The size of the address bus determines the maximum size of RAM
- The size of the data bus determines the maximum size of an operand in an instruction
- Pipelining is used to improve efficiency

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